(Amended) An input buffer circuit comprising:

a first inverting switch connected to a first input you tage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and outputting an output

signal;

a gain control unit having a feedback, loop for gain control and responding to the self bias

signal and the output signal.

(Amended) An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and outputting an output

signal;

a gain control unit having a feedback loop for gain control responsive to the self bias

signal and the output signal; and

a current controlling circuit that supplies current to the first inverting switch, the second

inverting switch and the gain control unit and sinks current from the first inverting switch, the

second inverting switch and the gain controlling circuit responding to the

self bias signal.

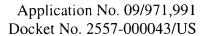
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(Amended) An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and outputting an ouput

signal;





a gain control unit having a feedback loop for gain control responsive to the self bias signal and the output signal; and

a swing width control circuit connected to a feedback signal that is inverted by the output signal.